Reduction of Leakage Current and Leakage Power during Write Operation Using Sleep Transistor in 6T, 8T, 10T SRAM

Siva Kumar.P[1], Jenyfal Sampson[2], Shabitha.S [3], Shenbaga Nivetha.K [4], Sindhu Bala.P [4],

[1] Associate Professor, [2] Assistant Professor II, [3][4][5]IV Year B. Tech,

Department of ECE, Kalasalingam University, Krishnankovil

E-mail: [1]siva@klu.ac.in,[2]jenyfal, [3][4][5] (shabisankar11, shenbaganivetha28,sindhubala) @gmail.com

Abstract- The aim of this paper is to reduce the maximum leakage current and power consumption using sleep transistors. In total power dissipation, the major dissipated portion is due to leakage power .When compared to stack approach in SRAM cell sleep transistor gives more advantages. This is used for research purpose and to do the operations of 6T, 8T, 10T with sleep transistor and our enhanced work is to implement a 16*8 matrix with sleep transistor in 6T SRAM cell design. The SRAM cell with 16*8 sleep transistor shows better leakage reduction for real time applications. In this paper Analog environment virtuoso (Tanner) simulator is used for analysis of the power associated with CMOS SRAM cell.

Index Terms—6T SRAM cell, Leakage power, Leakage current, 16*8 matrix and sleep transistor

I. INTRODUCTION

Leakage of current is decreasing day by day due to technology development. So, the several techniques are used for leakage reduction in CMOS digital integrated circuits[1]. This objective demonstrates the ideas of 6T, 8T, 10T models with sleep transistors. Sleep transistors are used in minimizing power consumption and heat dissipation. Leakage reduction can be done by 16*8 matrix in 6T SRAM using sleep transistor for real time applications like pen drive, memory card and hard disk. We are going to do the operations of 6T, 8T, 10T with sleep transistor [2]. The SRAM architecture is mainly used to the single cell storage process in any type of memory architecture. And the architecture require less power consumption for the storage of 1-bit.SRAM Design is focused on both Current and Leakage Power Performance and also Which solves the long discharging problem during the data transition[3]. The SRAM architecture consumes less energy due to the internal memory placement. In Proposed system, 16*8 matrix in 6T SRAM design using sleep transistor and to calculate how much power consumed in it. The sleep circuits reduce leakage power when these operate in "stand-by mode" due to inefficient passing of the voltages [4].

This paper is organized as follows. Section II gives the brief idea of the previous research on leakage for various SRAM models using sleep transistor, section III describes the SRAM model 6T, 8T and 10T using sleep transistor model. Section IV describes simulation. In section V, proposed low leakage SRAM model are shown. Here the leakage is reduced by 16*8 matrix in 6T SRAM using sleep transistor. In the section VI the result part is discussed and compares leakage power and time consumed for SRAM cells. The section VII demonstrates the conclusion of this paper and gives idea about sleep transistor for low leakage reduction [5].

II. PREVIOUS WORK

To optimize the data Leakage current and to reduce the power consumption [6]. In

previous work, designing 6T, 8T, 10T with sleep transistor based data storage architecture and to interchange the sleep transistor for 6T, 8T and 10T [7].In type I circuits in active mode, both sleep transistor are turned on and in type II circuits both sleep transistor are turned off. When the sleep transistor is turned off the circuit is called as stand-by mode. The result section of this paper shows that the leakage power is drastically reduced in the 16*8 sleep transistors as compared to the sleep approach.

The other techniques like forced sleep approach and sleep keeper approach are used to optimize the leakage reduction. The forced sleep approach is the best technique as it reduces almost 88% of sub threshold leakage power compared to sleep transistor.

III. CONVENTIONAL SRAM MODELS

Sleep transistors are the two extra transistors connected to the SRAM circuit. Two sleep transistors is used to reduce the leakage when compared to previous model.

A. 6T SRAM with Sleep Transistors

The leakage power can be reduced by adding two sleep transistors in 6T SRAM circuit. Both the PMOS (P3) and NMOS (N7) are the sleep transistors.[8].The type I circuit is shown in fig 1.In active mode both the sleep transistors are turned on. So, the PMOS (P3) is kept low and NMOS (N7) is kept high. According to pass transistor property the source node of two PMOS are at $V_{dd.}$ Similarly the source nodes of two NMOS are at 0.In standby mode both the sleep transistor (P3 and N7) are turned off.

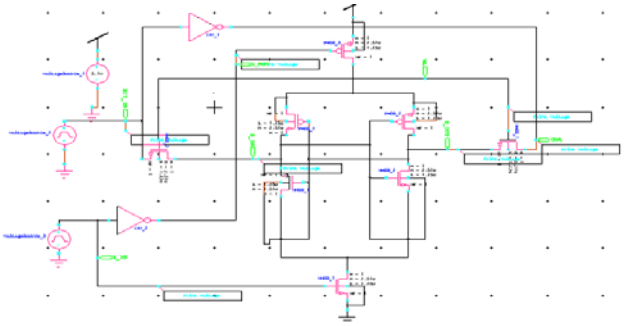


Figure 3.1.6T SRAM with sleep transistors (Type- I)

In type II NMOS (N7) and PMOS (P3) sleep transistors are interchanged. The modified circuit is shown in Figure 3.2

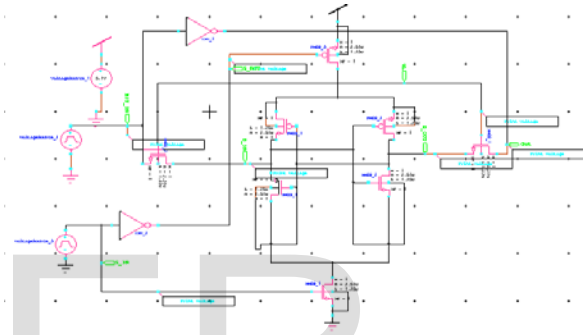


Figure 3.2. 6T SRAM with sleep transistor (Type II)

In type I both sleep transistor are turned on. According to pass transistor property the voltage at the source node of N7 would be V_{dd}-V_{th}, where as source node of P3 would be ~V_{th}. In stand-by mode both the sleep transistor are turned off. The high impedance path provided by the transistors between V_{dd} to ground and therefore, a sub-threshold leakage current flows.

B. 8T SRAM with sleep Transistors

In this section, two sleep transistors PMOS (P3) and NMOS (N5) are connected with pull-up networks (P1 and P2) and pull-down networks (N1 and N2) are shown in figure.3.3.In 8T the leakage reduction is due to increasing threshold voltage (V_{th}) and V_{th} increase due to NMOS (N6 and M10) transistors in stack effect of pull-down network.

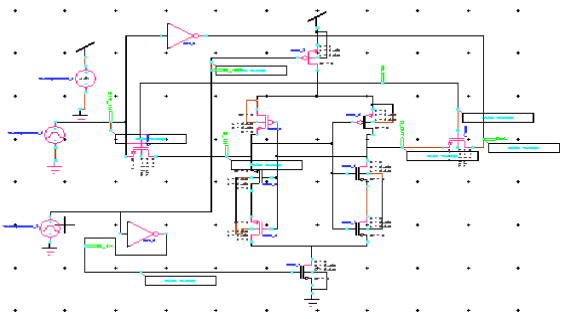


Figure 3.3 8T SRAM with sleep transistor (Type-I)

In type I circuit both the sleep transistor(P3 and N5) are turned on.P3 passes supply voltage(V_{dd}) and (N7) passes ground voltage (0).In standby mode both the sleep transistor are turned off and the leakage is reduced. When the word lines are high the operation will start[9].This circuit has reduced sub threshold leakage power.

Now in type II circuit both NMOS (N5) and PMOS (P3) are interchanged. In active mode both the sleep transistor are turned on.And the source voltage of NMOS(N5) will be ~(V_{dd}-V_{th}) and the source voltage of PMOS(P3) will be ~V_{th}. In standby operation load circuit is disconnected from supply voltage. So, due to higher impedance path between V_{dd} to ground a small subthreshold leakage current flows. This is called forced sleep technique.

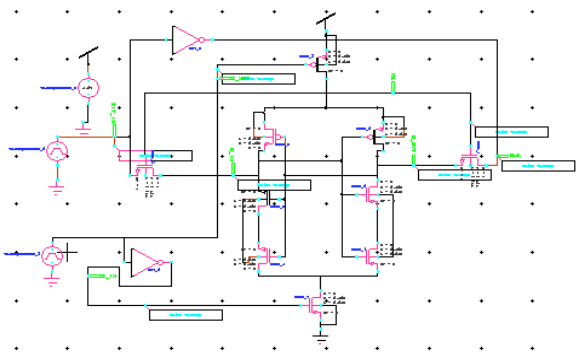


Figure 3.4.8T SRAM with sleep transistor (Type- II)

C. 10T SRAM with sleep transistor

In this section two PMOS (P4 and P5) transistors and two NMOS (N5 and N6) transistors are connected in stack form. Here eight cross-coupled transistors connected serially and two sleep transistors (P3 and N7).

In type I circuit PMOS sleep transistor (N7) connected between supply voltage and NMOS (P3) sleep transistor is connected between SRAM load and ground terminal. The circuit is shown in Figure 3.6. In active mode both the sleep transistor are turned on. The drain node of (N7) becomes 1 and drain node of (P3) becomes 0.In standby mode both the sleep transistors are turned off. So the load circuit is disconnected from the supply voltage and ground. Thus the small leakage current flows in 10T type I mode.

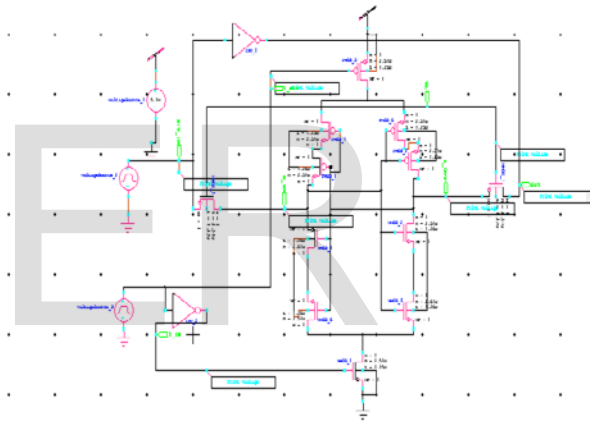


Figure 3.5.10T SRAM with sleep transistor (Type-I)

In type II, the NMOS sleep transistor (P3) is connected to V_{dd} and PMOS sleep transistor (N7) is connected to ground. During active mode both the sleep transistor are turned on. So the NMOS transistor (P3) is connected to V_{dd}. In sleep mode it is not possible in giving V_{dd} and so the inputs are low, the output voltage is reduced to ~(V_{dd}-V_{th}).The PMOS (N7) is grounded. When the input signal is high the output is ~V_{th}. Thus the leakage current flow through the transistor is reduced.[10]

Circuit	Total leakage power (Micro watts)	Time Taken (nano seconds)
6T SRAM with sleep transistor type I	90	5.57
8T SRAM with sleep transistor type I	85	5.91
10T SRAM with sleep transistor type I	90	5.57
6T SRAM with sleep transistor type II	120	6.26
8T SRAM with sleep transistor type II	120	6.26
10TSRAM with sleep transistor type II	120	5.57

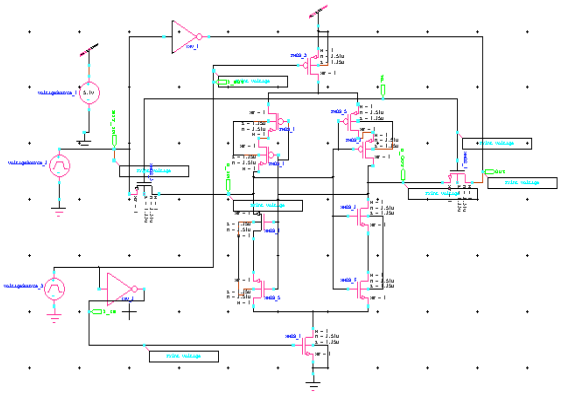


Figure 3.6.10T SRAM with sleep transistor (Type -II)

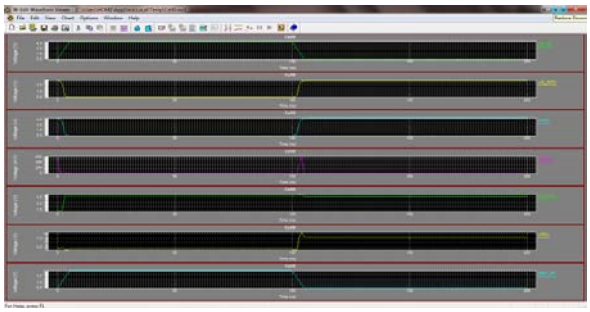
TABLE I

Comparison of Leakage power for Various SRAM Cell

Here we compare 6T, 8T and 10T leakage power. From the above table 6T type I is found to be better than other methods, based upon the power-time taken product. So we proposed 6T SRAM cell for memory array.

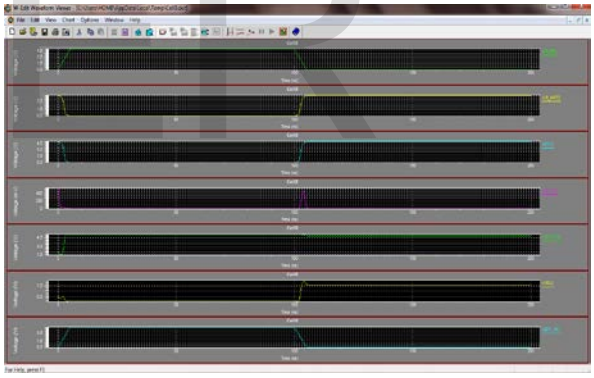
IV. SIMULATION AND RESULT

6T (Type-I):



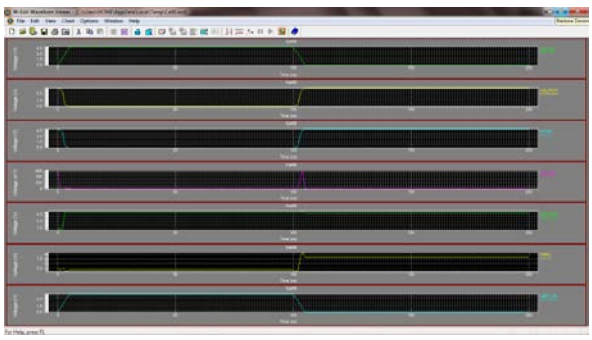
This waveform shows the Bit line ,write operation and sleep transistor output.

8T (Type-I):



This waveform shows the Bit line, write operation and sleep transistor output

10T (Type-I);



This waveform shows the Bit line, write operation and sleep transistor output.

V.PROPOSED LOW LEAKAGE SRAM CELL

In this section we have designed 6T SRAM cell using sleep transistor in 16*8 matrix.

6T SRAM Cell using Sleep transistor in 16*8 Matrix:

We have designed 6T with 16*8 matrix using sleep transistor.16*8 matrix will reduce the leakage than previously design 6T with sleep transistor. [11]. Memory arrays are an essential building block in any digital system.[12]Design choices were made and justified appropriately.[13].

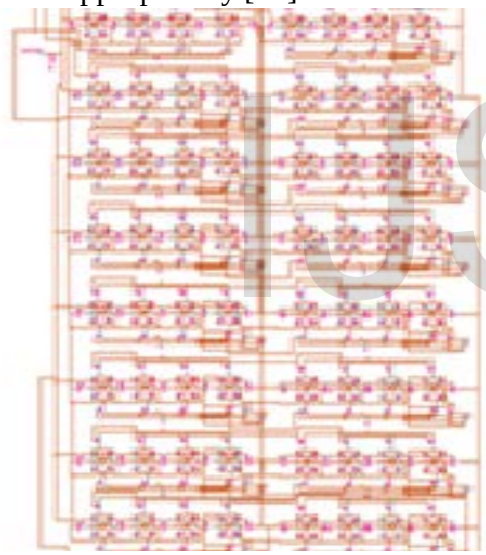


Figure 4.1 16*8 matrix in 6T SRAM using Sleep Transistor

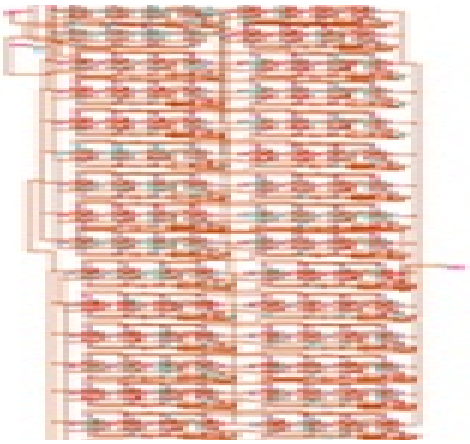


Figure 4.2 16*8 matrix in 6T SRAM using Sleep Transistor

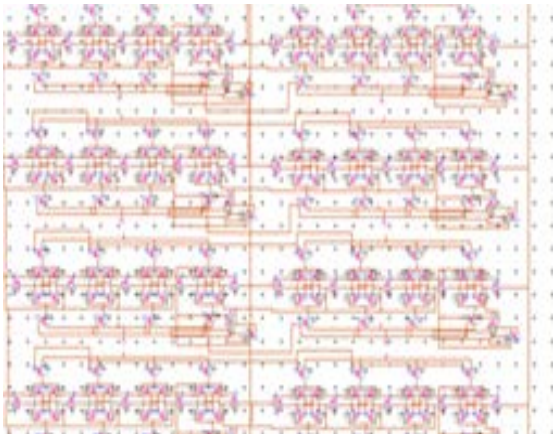
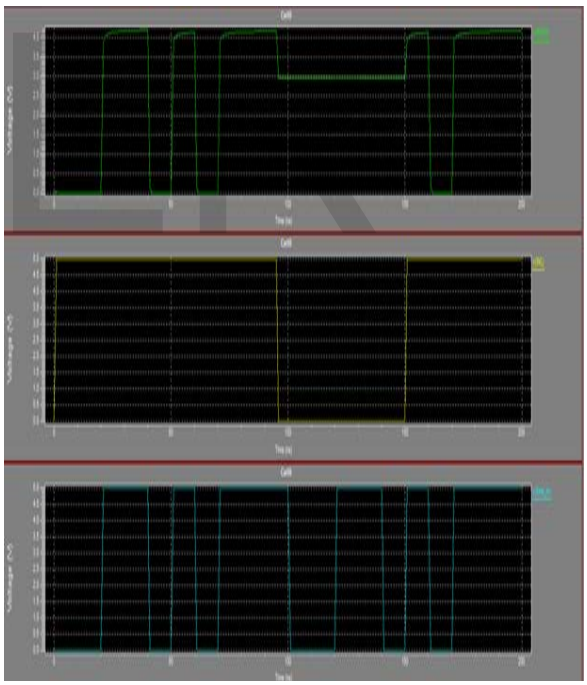


Figure 4.3 16*8 matrix in 6T SRAM using Sleep Transistor

OUTPUT:



VI.RESULT AND DISCUSSIONS

In this paper Tanner 13.0 is used to find out the leakage power and leakage current in CMOS SRAM cell technology. Table shows the leakage current in 6T, 8T and 10T SRAM cell using sleep transistor. From the table 6T SRAM type I using sleep

transistor shows the better leakage than other techniques. Similarly in 6T using 16*8 matrix using sleep transistor shows better performance in real life application.

VII.CONCLUSION

Study of result show that 6T type I is the best technique in sleep transistor. Using this 6T SRAM using sleep transistor 16*8 matrix we have reduced the leakage power. In this paper as the number of transistors increase (8T, 9T and l0T) leakage power reduces but area and delay also increase more and more. Hence the authors conclude the proposed SRAM circuits specially type-I circuit, used for low power designs can be used for low power applications.

VIII.ACKNOWLEDGEMENT

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